REMARKS/ARGUMENTS

Request for Continued Examination:

The applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

Claims 1-3, 5-11, 13-44, and 83-94 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-53 and 78-95 of copending application No. 10/707,871 in view of Bicknell et al. (US pub. 2003/0193776).

The applicant asserts that claims 1-3, 5-11, 13-44, and 83-94 should not be found unpatentable under double patenting because the Examiner failed to show that the cited reference teaches both element A AND element B in his/her claim rejection in the current OA. This is because the correct relationship between elements A & B is AND according to claim 1, and not OR, as was utilized by the Examiner (see claim 1).

Regarding independent claim 1, for example, the claim language includes the feature, "bringing the LMU on line while the JBOD emulation controller is on line, **and** taking the LMU off line while the JBOD emulation controller is on line" (emphasis added) However, on page 6 of the Office action, fourth line from the bottom, the Examiner stated that Bicknell et al. discloses "bringing the LMU on line **or** taking the LMU off line while the JBOD emulation controller is on line". (Emphasis added)

The applicant again notes that the claim language utilized in the present invention is "and", and therefore, the present invention performs both the claimed functions of "bringing the LMU on line" and also "taking the LMU off line".

However, in the Office action, the Examiner utilized "or" stating that Bicknell discloses, "bringing the LMU on line" or "taking the LMU off line". In other words, only one of these functions is performed by the prior art. Furthermore, Bicknell paragraph 0019 only mentions "Disc drive 106 can preferable be removed without disturbing the operation of subsystem 100"; however, the applicant points there is no mention of "bringing the LMU on line" by Bicknell.

For at least these reasons, the applicant asserts that claim 1 should not be found unpatentable over copending application No. 10/707,871 in view of Bicknell et al. (US pub. 2003/0193776). Withdrawal of the double patenting rejection in view of these arguments is respectfully requested.

Claims 1-3, 5-9, 11, 13-17, 24-29, 31-35, 38-40, 44, 83, 84, and 86-93 are rejected under 35 USC 103a as being unpatentable over Bicknell et al. (US Pub. 2003/0193776) in ivew of Meehan et al. (US pub. 2004/0177218) and further in view of Sebastian et al. (US pub. 2004/0083308).

The applicant has amended the claims to remove the non-limiting intended use term "is capable of". For example, line 10 of claim 1 is amended to change "is capable of performing" to "performs". In this way, the components are described both in terms of their structure and also in terms of their function. Similar amendments to other claims removing "is capable of" are made as shown above. Additional amendments are made to change "set" to "group" and to correct various antecedent basis issues discovered during the drafting of this response to Office action. No new matter is entered.

Independent claims 1, 8, 83, and 92

Concerning the patentability of currently amendment independent claim 1, firstly, as was emphasized above, the claim language includes the feature, "bringing the LMU on line while the JBOD emulation controller is on line, **and** taking the LMU off line while the JBOD emulation controller is on line" (emphasis added) However, on page 6 of the Office action, fourth line from the bottom, the Examiner stated that Bicknell et al. discloses "bringing the LMU on line **or** taking the LMU off line while the JBOD emulation controller is on line". (Emphasis added)

The applicant again notes that the claim language utilized in the present invention is "and", and therefore, the present invention performs both the claimed functions of "bringing the LMU on line" and also "taking the LMU off line".

However, in the Office action, the Examiner utilized "or" stating that Bicknell discloses, "bringing the LMU on line" or "taking the LMU off line". In other words, only one of these functions is performed by the prior art. Furthermore, Bicknell paragraph [0019] only mentions "Disc drive 106 can preferable be removed without disturbing the operation of subsystem 100", however, the applicant points there is no mention of "bringing the LMU on line" by Bicknell.

Secondly, on page 10 of the Office action, the Examiner admitted that "Neither Bicknell nor Meehan specifically discloses a RAID controller being use as JBOD controller. Sebastian specifically discloses a RAID controller being use as JBOD controller (see paragraph 0050)". However, the applicant respectively disagrees. Paragraph [0050] of Sebastian only states, "Each storage device 510 can be a storage

array using SCSI, PCI-X or other bus architecture, JBOD(Just a Bunch of Disks), a RAID (Redundant Array of Inexpensive Disks) enclosure, or other mass storage device."Such teachings are in contrast to the present invention independent claims stating "JBOD emulation controller". An important point is that "JBOD" is not equivalent to a "JBOD emulation controller". For example, please refer to Figure 3 showing a subsystem according an exemplary embodiment of the present invention. Element 38 is the "JBOD emulation controller", while the JBOD is simply the storage device formed by the plurality of PSDs 36.

In summary, for at least the above two reasons, the applicant asserts that claim 1 of the present invention should be found allowable in view of the cited references because none of the cited references, alone or in combination, teach each and every feature claimed. Similar arguments also apply to independent claims 8, 83, and 92; and the various dependent claims should also be found allowable for at least the same reasons as their respective base claims. Reconsideration of claims 1-3, 5-9, 11, 13-17, 24-29, 31-35, 38-40, 44, 83, 84, and 86-93 in view of these arguments is respectfully requested. Further comments regarding the patentability of particular dependent claims with respect to the cited references are provided in the below paragraphs.

Regarding claims 13, 86 and 89

The instant application claims "comprising **auto-on-lining mechanism** to automatically bring on line a said LMU which was previously off-line once **a requisite quorum of said PSDs** comes on-line."

What is the quorum? Please refer to paragraph [0075] of the present invention,

in which "A quorum herein means a group of one or more member drives of an LMU to which data can be accessed correctly by the subsystem. For example, in RAID 0, a quorum comprises all the member disk drives of an LMU; in RAID 1, a quorum comprises at least one of the mirrored disk drive pair in every mirrored disk drive pair of an LMU; and, in RAID 3 through 5, a quorum comprises at least all but one of the member disk drives of an LMU." From aforesaid descriptions, it can be concluded as follows:

In RAID 0 (striping), a quorum comprises every member disk drives of an LMU.

In RAID 1 (mirroring), a quorum comprises at least one of the mirrored disk drive pair in every mirror disk drive pair of an LMU.

In RAID 3 to 5, a quorum comprises at least all but less one of the member disk drives of an LMU.

In other words, number of disk drives must reach "quorum" so that different RAID levels can work and function.

No matter what RAID level it is, as soon as quorum of disk drives of LMU is reached (for example, insertion of disk drive), the LMU is automatically brought on-line. On the other hand, as soon as quorum of disk drives of LMU is not reached (for example, removal of disk drive), the LMU is automatically brought off-line.

In addition, **what is the auto-on-lining mechanism of the present invention?** Please refer to paragraph [0076] and [0077] of the present invention in which [0076]

An important enabling element of the automated on-lining and off-lining of LMUs in response to PSD insertions/removals is a facility for detecting if a PSD 36 is inserted/removed into/from the JBOD enclosure. FIG. 15 shows an example of such a detection facility. The JBOD emulation controller 38 monitors the state of this detection facility to determine when a PSD 36 is removed or inserted. In the simplest case, in which each logical media unit is composed of a single PSD, removal of the PSD will trigger the initiation of the procedure that takes the corresponding logical media unit off line, while insertion will trigger the procedure to scan in and then bring on line the corresponding logical media unit, and [0077]in order to support the above-mentioned features of the present invention JBOD subsystem, the JBOD subsystem can further comprises an auto-on-lining mechanism to automatically bring on line a said logical media unit which was previously off-line once a requisite quorum of said PSDs comes on-line, an auto-off-lining mechanism to automatically take off line a said logical media unit which was previously on-line once a requisite quorum of said PSDs becomes off-line, a determining mechanism for automatically determining when a PSD has been removed or when one has been inserted, and a scanning-in mechanism to automatically scan in PSDs on detection of insertion of the PSDs. The present invention indeed discloses structures regarding how insertion/removal of PSD 36 into/from the JBOD enclosure is detected by a detecting facility. FIG. 15 shows an example of such a detection facility. The JBOD emulation controller 38 monitors the state of this detection facility to determine when a PSD 36 is removed or inserted.

In contrast, paragraph 0030 of Bicknell does not disclose the auto-on-lining

mechanism and quorum at all, and thus fails to disclose to "comprising **auto-on-lining mechanism** to automatically bring on line a said LMU which was previously off-line once **a requisite quorum of said PSDs** comes on-line.".

From the aforesaid explanations and descriptions, all prior arts have never taught or suggested all independent claims of the instant application and thus all independent claims are in condition for allowance. Since all independent claims of the instant application are in condition for allowance, the dependent claims which depend on the independent claims, should be allowable, too.

Regarding dependent claims 14, 87 and 90

The instant application claims "comprising auto-off-lining mechanism to automatically take off a said LMU which was previously on-line once a requisite quorum of said PSDs becomes off-line."

The meaning of "quorum" is explained in detail as aforesaid and thus is omitted here.

In addition, what is the auto-off-lining mechanism of the present invention?

Please refer to paragraphs [0076] and [0077] of the present invention in which [0076] An important enabling element of the automated on-lining and off-lining of LMUs in response to PSD insertions/removals is a facility for detecting if a PSD 36 is inserted/removed into/from the JBOD enclosure. FIG. 15 shows an example of such a detection facility. The JBOD emulation controller 38 monitors the state of this

detection facility to determine when a PSD 36 is removed or inserted. In the simplest case, in which each logical media unit is composed of a single PSD, removal of the PSD will trigger the initiation of the procedure that takes the corresponding logical media unit off line, while insertion will trigger the procedure to scan in and then bring on line the corresponding logical media unit, and [0077] in order to support the above-mentioned features of the present invention JBOD subsystem, the JBOD subsystem can further comprises an auto-on-lining mechanism to automatically bring on line a said logical media unit which was previously off-line once a requisite quorum of said PSDs comes on-line, an auto-off-lining mechanism to automatically take off line a said logical media unit which was previously on-line once a requisite quorum of said PSDs becomes off-line, a determining mechanism for automatically determining when a PSD has been removed or when one has been inserted, and a scanning-in mechanism to automatically scan in PSDs on detection of insertion of the PSD. Again, the present invention indeed discloses structures regarding how insertion/removal of PSD 36 into/from the JBOD enclosure is detected by a detecting facility. FIG. 15 shows an example of such a detection facility. The JBOD emulation controller 38 monitors the state of this detection facility to determine when a PSD 36 is removed or inserted.

In contrast, paragraph 0019 of Bicknell only discloses "Disc drive 106 can preferably be removed without disturbing the operation of subsystem 100", but fail to teach or suggest "such an auto-off lining mechanism of the present invention to automatically take off line logical media unit."

Regarding dependent claim 16

The instant application claims "comprising scanning-in mechanism to automatically scan in PSDs on detection of insertion of the PSD." Please refer to [0077] of the present invention in which [0077] in order to support the above-mentioned features of the present invention JBOD subsystem, the JBOD subsystem can further comprises an auto-on-lining mechanism to automatically bring on line a said logical media unit which was previously off-line once a requisite quorum of said PSDs comes on-line, an auto-off-lining mechanism to automatically take off line a said logical media unit which was previously on-line once a requisite quorum of said PSDs becomes off-line, a determining mechanism for automatically determining when a PSD has been removed or when one has been inserted, and a scanning-in mechanism to automatically scan in PSDs on detection of insertion of the PSD. That is, the scanning-in mechanism of the present invention automatically scan in PSDs upon detection of insertion of the PSD.

In contrast, paragraph 0003 of Bicknell only discloses "an electrical connection with the midplane card for data communication with the disc drives", but fails to teach or suggest "such a scanning-in mechanism" at all, not to speak of "automatically scanning in PSDs on detection of insertion of the PSD" of the present invention.

Regarding dependent claim 17

The instant application claims "comprising information mechanism for informing the host entity when the mapping of said LMUs to host-side interconnect LUNs has changed." Please refer to paragraph 0079 of the present invention, in which [0079] In

general, when the mapping of LMUs to the host-side IO device interconnect LUNs has changed, either when an LMU is newly introduced onto the Fibre loop or when an existing LMU is removed therefrom, the host entity will be informed of such change. An example of such JBOD emulation controller is that when the host-side IO device interconnect is a Fibre operating in Arbitrated Loop mode, while the external JBOD emulation controller can issue a LIP when a new target ID is introduced onto the Fibre loop or is removed from the Fibre loop so as to inform other devices on the loop that the loop device map has changed. Another example is that when the JBOD emulation controller support standard SCSI command set as a primary command interface with the host entity over the host-side IO device interconnect, the JBOD emulation controller posts a status of "CHECK CONDITION" to the host entity with sense key of "UNIT ATTENTION" and sense code of "REPORTED LUNS DATA HAS CHANGED" to inform the host entity when the mapping of LMUs to the host-side IO device interconnect LUNs has changed. That is, for example, when an LMU is newly introduced onto the Fibre loop or when an existing LMU is removed therefrom, i.e., the mapping of LMUs to the host-side IO device interconnect LUNs has changed, the host entity will be informed of such a change of mapping of LMUs to the host-side interconnect LUNs. In other words, change of mapping depends on insertion/removal of the LMU. Upon insertion/removal of the LMU, change of mapping to the host-side IO device interconnect LUNs happens.

In contrast, paragraph 0017 of Bicknell only discloses "Each intermediate electronic component 110 determines which controller 108 is provided data access to a particular disc drive 106 by opening and closing data communication paths between

the disc drive 106 and each of the controller 108. In the event that one of the controller 108 fails, data stored in the disc drives 106 can still be accessed by the host computer through the remaining active controller 108. In this manner, the reliability of disc storage subsystem 100 is improved", but fails to teach or suggest "informing the host entity when the mapping of said LMUs to host-side interconnect LUNs has changed." of the present invention."

Regarding original claim 32

Original claim 32 of the instant application claim "comprising an enclosure management services mechanism." Please refer to [0093] of the instant application in which "Yet another feature of a JBOD subsystem is enclosure management services (EMS). This is an intelligent circuitry **that monitors status of various enclosure devices, such as power supplies, fans, temperatures, etc. and can be interrogated by a host for these statuses.**" That is, The instant application claims comprising an enclosure management services (EMS) mechanism, in which the EMS mechanism is an intelligent circuitry that monitors status of various enclosure devices, such as power supplies, fans, temperatures, etc. and can be interrogated by a host for these statuses.

In contrast, paragraph 0037 of Bicknell only discloses "the multiplexing electronics selectively opens and closes the first and second data communication paths in response to at least one control signal (such as 218 or 220)". Mux can not perform the functions the EMS mechanism like **monitoring status of various enclosure devices, such as power supplies, fans, temperatures, etc. power supplies, fans,**

temperatures, etc. In other words, **obviously, MUX 208 of Bicknell is not equal to the EMS of the present invention, and naturally** fails to disclose, such as the **EMS mechanism which is an intelligent circuitry that monitors status of various enclosure devices, such as power supplies, fans, temperatures, etc. power supplies, fans, temperatures, etc.**

Since all independent claims of the instant application are in condition for allowance, all dependent claims which depend on the independent claims should be allowable, too.

Claims 36 and 37, are rejected under 35 USC 103a as being unpatentable over Bicknell et al. (US Pub. 2003/0193776) in ivew of Meehan et al. (US pub. 2004/0177218) and Sebastian et al. (US pub. 2004/0083308) as applied to claim 32, and further in view of Rabinovitz et al. (US pat. 6,483,107).

As was stated above, claims 36 and 37 are dependent upon base claim 8 through several intervening claims all believed allowable for at least the above stated reasons. Therefore, claims 36 and 37 should be found allowable for at least the same reasons. Reconsideration of claims 36 and 37 is respectfully requested.

Claims 18-23 and 30, are rejected under 35 USC 103a as being unpatentable over Bicknell et al. (US Pub. 2003/0193776) in ivew of Meehan et al. (US pub. 2004/0177218) and Sebastian et al. (US pub. 2004/0083308) as applied to claim 8,

and further in view of Watanable (US pub. 2004/0260873).

Regarding dependent claim 18

The instant application claims comprising unique ID determination mechanism to uniquely identify said PSDs independent of their location in which they are installed in the JBOD subsystem. Please refer to [0086] of the instant application, in which "In other embodiment of the present invention, the JBOD subsystem can also comprise an unique ID determination mechanism to uniquely identify said PSDs independent of their location in which they are installed in the JBOD subsystem. wherein information used to uniquely identify each of said PSDs can be stored on the PSD. LMU identification and configuration information can be stored on the member PSDs that compose the LMU." That is, the unique ID determination mechanism is used to uniquely identify said PSDs independent of their location in which they are installed in the JBOD subsystem. Once previously removed PSD that is previously provided with the unique ID, is re-inserted into the JBOD subsystem, the unique ID determination mechanism can uniquely identify said PSDs through the unique ID independent of their location, i.e., does not relate to the location into which the previously removed PSD is inserted.

In contrast, paragraph 0114 of Watanable only discloses "each volume 1101a-c is assigned to the physical port 1103a-c which is addressable on a storage I/O interface (e.g., IO I/F 331 of FIG.3) when a volume is accessed from a host (e.g., host 301).", but fail to teach "to uniquely identify said PSDs independent of their location in which they are installed in the JBOD subsystem."

Regarding dependent claim 23

The instant application claims "LMU identification information presented to the host entity is generated as follows: from information stored in a non-volatile memory in the JBOD subsystem prior to being able to obtain LMU identification information off of the member PSDs and from LMU identification information stored on the member PSDs that compose the LMU after the member PSDs become accessible".

Please refer to paragraph [0083] of the instant application, in which "If a PSD whose identification information has already been stored to non-volatile memory as above has failed or is removed from the JBOD emulation SV subsystem while the subsystem is in a powered-down state and then the subsystem is subsequently powered up, during power-up initialization process and prior to being able to determine that the PSD is not present and/or its identification information not accessible, the SVC may present the original PSD's identification information to the host. Only after the SVC finally determines that the PSD is not present or no longer accessible will it discover that it has presented the wrong information to the host. At this point, the JBOD emulation SV subsystem would typically emulate a PSD removal in an attempt to alert the host that it should re-scan the PSD", and to paragraph [0084] of the instant application, in which "<u>If a new PSD is inserted into a powered-down SV subsystem and the subsystem is subsequently powered up, the new PSDs identification information will still remain unavailable until the SVC is able to successfully read the information from the reserved space on the PSD</u>, so a relatively extended latency will be incurred. If the PSD has never been configured before such that it does not have any identification or configuration information stored on it, the JBOD emulation SV subsystem may elect to ignore it, requiring that each usable PSD

must be pre-configured (e.g., factory configured), or it may generate a set of identification and configuration information for the PSD and store it to reserved space on the PSD, at the same time, making a copy to non-volatile memory. If the newly inserted PSD does have identification and configuration information already written on it, then the appropriate information would be copied to non-volatile memory. If there was no previous identification information associated with the particular host-side interconnect ID/LUN, then the JBOD emulation SV subsystem would simply alert the host(s) to rescan the interconnect for new PSDs. If, on the other hand, the host-side interconnect ID/LUN to be associated with the new PSD is identical to the ID/LUN associated with a PSD that has been removed or otherwise is no longer active, the SVC may already have a record of the original PSD and associated identification information in non-volatile memory. During power-up initialization, prior to being able to successfully read the identification information off of the new PSD, the SVC may end up presenting the original PSD's identification information to the host. Only after the SVC finally reads the information off of the new PSD will it discover that it has presented the wrong information. At this point, the JBOD emulation SV subsystem would typically emulate a PSD removal followed by an insertion in an attempt to alert the host that it should re-scan the PSD." From the above descriptions, it can be concluded (1) that prior to being able to obtain LMU identification information off of the member PSDs, LMU identification information presented to the host entity is generated from information stored in the non-volatile memory in the JBOD subsystem, and (2) that after the member PSDs become accessible, LMU identification information presented to the host entity is generated

from LMU identification information stored on the member PSDs that compose the LMU. That is, how to obtain LMU identification information depends on whether the member PSDs become accessible or not, which is the key point of obtaining the LMU identification information.

In contrast, paragraphs 0065, 0094, and 0114 of Watanable only disclose assignment of ID to the host, "input, intermediate or resulting data or functional elements can further reside more transitionally or more persistently in a storage media, cache or other volatile or non-volatile memory, (e.g. storage device 307 or memory 308) in accordance with a particular application", and "each volume 1101a-c is assigned to the physical port 1103a-c which is addressable on a storage I/O interface (e.g., IO I/F 331 of FIG. 3) when a volume is accessed from a host (e.g., host 301). Each volume is also assigned a unique ID 1104a-c, for example a WWN reference for fiber channel, a SCSI name for iSCSI, and so on.", but **fail at all to teach or suggest where to obtain the LMU identification information before being able to obtain LMU identification information off of the member PSDs, and where to obtain the LMU identification information after the member PSDs become accessible.**

Claim 42, is rejected under 35 USC 103a as being unpatentable over Bicknell et al. (US Pub. 2003/0193776) in ivew of Meehan et al. (US pub. 2004/0177218) and Sebastian et al. (US pub. 2004/0083308) as applied to claim 9, and further in view of Colton (US pub. 2005/0089027).

As was stated above, claim 42 is dependent upon base claim 8 through several intervening claims all believed allowable for at least the above stated reasons.

Therefore, claim 42 should be found allowable for at least the same reasons. Reconsideration of claim 42 is respectfully requested.

New Claims 95-109

New dependent claims 95-109 are added. No new matter is entered. Comments regarding the patentability of the new claims are provided in the below sections.

Regarding new claims 95, 99, 102 and 106

New claims 95, 99, 102 and 106 of the instant application claim "wherein said external JBOD emulation controller is adapted for accommodating said group of PSDs of different serial protocols." Said SVCs are adapted for accommodating said group of PSDs of different serial protocols i.e., SAS PSD and SATA PSDs.

In contrast, the applicant asserts that all cited references fail to teach or suggest "said SVCs are adapted for accommodating said group of PSDs of different serial protocols."

Regarding new claims 97, 101, 104, and 108

New claims 97, 101, 104, and 108 of the instant application claim "wherein said JBOD emulation controller issues a device-side IO request to said IO device interconnect controller, and said IO device interconnect controller re-formats said device-side IO request and accompanying IO data into at least one data packet for transmission to said group of PSDs through said device-side IO device interconnect port, wherein said data packet comprises a start segment at the beginning indicating

the start of said data packet, an end segment at the end indicating the end of the data packet, a payload data segment containing actual IO information to transmit through the SAS device-side IO device interconnect port, and a check data segment containing check codes derived from said payload data for checking the correctness of said payload data after transmission." In addition, take claim 97 for example, "wherein said data packet comprises a start segment at the beginning indicating the start of said data packet, an end segment at the end indicating the end of the data packet, a payload data segment containing actual IO information to transmit through the device-side IO device interconnect, and a check data segment containing check codes derived from said payload data for checking the correctness of said payload data after transmission.". that is, according to the independent claims of the present invention, the present invention re-formats said device-side IO request and accompanying IO data into at least one data packet, in which the data packet comprises the start segment for indicating the start of said data packet to be transmitted, the end segment for indicating the end of the data packet to be transmitted, the payload data segment containing actual IO information to be transmitted, and check data segment containing check codes for checking the correctness of said payload data after transmission (please refer to Fig.10 and paragraphs 0061 and 0065 of the present invention).

In contrast, the applicant asserts that all cited references fail to teach or suggest the following (a), (b), (c) and (d). i.e., the data packet comprises (a) the start segment for indicating the start of said data packet to be transmitted, (b) the end segment for indicating the end of the data packet to be transmitted, (c) the payload data segment containing actual IO information to be transmitted, and (d) check data segment

containing check codes for checking the correctness of said payload data after transmission.

Regarding New claims 98, 105 and 109

New claims 98, 105 and 109 of the instant application claim "comprising an enclosure management services mechanism." Please refer to [0093] of the instant application in which "Yet another feature of a JBOD subsystem is enclosure management services (EMS). This is an intelligent circuitry **that monitors status of various enclosure devices, such as power supplies, fans, temperatures, etc. and can be interrogated by a host for these statuses.**" That is, The instant application claims comprising an enclosure management services (EMS) mechanism, in which the EMS mechanism is an intelligent circuitry that monitors status of various enclosure devices, such as power supplies, fans, temperatures, etc. and can be interrogated by a host for these statuses.

In contrast, paragraph 0037 of Bicknell only discloses "the multiplexing electronics selectively opens and closes the first and second data communication paths in response to at least one control signal (such as 218 or 220)". Mux can not perform the functions the EMS mechanism like **monitoring status of various enclosure devices, such as power supplies, fans, temperatures, etc. power supplies, fans, temperatures, etc.** In other words, **obviously, MUX 208 of Bicknell is not equal to the EMS of the present invention, and naturally** fails to disclose, such as the **EMS mechanism which is an intelligent circuitry that monitors status of various enclosure devices, such as power supplies, fans, temperatures, etc. power supplies,**

fans, temperatures, etc.

Conclusion

Thus, all pending claims are submitted to be in condition for allowance with respect to the cited art for at least the reasons presented above. The Examiner is encouraged to telephone the undersigned if there are informalities that can be resolved in a phone conversation, or if the Examiner has any ideas or suggestions for further advancing the prosecution of this case.

Sincerely yours,

/Winston Hsu/ Date: 01/20/2009

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)